In the claims:

Please amend the claims as follows:

1-14 (Cancelled)

14-20 (Withdrawn)

21. (Currently Amended) A method for fabricating a metallization arrangement for a semiconductor structure, said method comprising:

providing a first [~~substructure~~] metallization plane on said semiconductor structure;

providing a first intermediate dielectric on said first [~~substructure~~] metallization plane;

providing a liner layer made of a dielectric material on said first intermediate dielectric [~~substructure plane~~];

providing via holes in said first intermediate dielectric and said liner layer, said via holes being filled with a conductive material, thereby completing a first resulting structure;

providing a second metallization plane on said first resulting structure;

patterning a first interconnect in said second metallization plane;

patterning a second interconnect in said second metallization plane;

interrupting said liner layer between said first interconnect and said second interconnect, thereby forming an interspace between said first and second interconnects.

22. (Previously Added) The method as claimed in claim **21**, wherein patterning and interrupting are carried out in a common etching step.

23. (Previously Added) The method as claimed in claim **21**, further comprising providing an electrical circuit integrated into a silicon substrate.

24. (Previously Added) The method as claimed in claim **23**, wherein providing a liner layer comprises fabricating said liner layer from a material selected from the group consisting of silicon dioxide and silicon nitride.

25. (Previously Added) The method as claimed in claim **24**, wherein said patterning is carried out in a first metal etching step and said interrupting is carried out in a second silicon dioxide etching step.

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26. (Previously Added) The method as claimed in claim **21**, further comprising providing a dielectric in said interspace.

27. (Currently Amended) The method as claimed in claim **21**, further comprising providing a mask on said second metallization plane for use in patterning and interrupting.

In the drawings:

Please substitute the enclosed FIG. 2 for the FIG. 2 presently in the application. The enclosed FIG. 2 is labeled as prior art, consistent with the Examiner's suggestion.